Notice of Allowability	Application No.	Applicant(s)	
	09/650,726	MIGLIANICO, DENIS	
	Examiner	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment received 7/24/06*.

2. ☒ The allowed claim(s) is/are *1-3 and 5-10, now renumbered as 1-9*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20060918* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

1. This communication is in response to Applicant's Amendment to Office Action dated March 23, 2006, mailed July 24, 2006, and telephone interview discussed on August 25, 2006.

1-1. Claims 1, 2, 5, 8, and 10 have been amended. Claims 12-14 have been added and then canceled. Claims 1-3 and 5-10 are pending.

1-2. Claims 1-3 and 5-10 have been examined and allowed.

EXAMINER'S AMENDMENT

2. An Examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to Applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. Authorization for this Examiner's amendment was given in a telephone interview with Mr. Diallo T. Crenshaw (Reg. No. 52,778) on September 18, 2006.

4. The title has been amended as follows:

A METHOD AND APPARATUS FOR TESTING THE OPERATION OF AN ELECTRONIC UNIT BY SIMULATION~~, AND AN INSTALLATION FOR TESTING A UNIT FOR FITTING TO A RAIL VEHICLE OR TO AN ELECTRIC VEHICLE~~

5. The claims have been amended as follows:

5-1. Replace claim 1 as follows:

1. (currently amended): A method of testing the operation of an electronic unit by stimulating

said unit with simulated input signals to said unit, the method comprising:

- sending simulated input signals to said unit and receiving slow output signals from said unit in response to said simulated input signals by at least one microprocessor;

- receiving fast output signals in response to said simulated input signals by at least one programmable logic circuit; ~~and~~

- processing the fast output signals by the at least one programmable logic circuit to generate parameter values at a first frequency;

- storing said parameter values corresponding to said processed signals in a storing circuit; and

- accessing said stored parameter values by the at least one microprocessor at a second frequency which is slower than said first frequency and is compatible with an operating frequency of the microprocessor that generates said simulated input signals,

wherein said at least one programmable logic circuit is of a field programmable gate array type.

5-2. Replace claim 5 as follows:

5. (currently amended): An apparatus for testing the operation of an electronic unit by simulation, said unit generating logic signals at specific instants, said apparatus comprising a simulator which comprises:

- at least one microprocessor sending simulated input signals to said unit and receiving slow output signals from said unit in response to said simulated input signals;

- at least one programmable logic circuit which receives at least one of fast output signals from said unit, said at least one programmable logic circuit processing the fast output

signals to generate, at a first frequency, parameter values corresponding to the fast output signals; and

- a storing circuit which stores said parameter values, wherein said microprocessor accesses said stored parameter values at a second frequency which is slower than said first frequency and is compatible with an operating frequency of said microprocessor,

wherein said at least one programmable logic circuit is of a field programmable gate array type.

5-3. Replace claim 8 as follows:

8. (currently amended): ~~The~~ An apparatus according to claim ~~5~~6, wherein said at least ~~one programmable logic circuit and said at least~~ one second programmable logic circuit is of the field programmable gate array type.

5-4. Replace claim 10 as follows:

10. (currently amended): ~~The~~ An apparatus according to claim 6, wherein said at least one programmable logic circuit and said at least one second programmable logic circuit is programmed as a function of ~~the~~ a type and/or intended use of said unit.

5-5. Cancel claims 12-14.

Reasons for Allowance

6. The following is an Examiner's statement of reasons for allowance:

6-1. The closest prior art of record discloses:

(1) A hardware-in-the-loop simulation to validate ECUs (Hanselmann, "Real-Time Simulation Replaces Test Drives").

(2) An integrated and flexible hardware and software environment for electric drives control (Bielewicz et al., "A DSP and FPGA Based Integrated Controller Development Solutions for High Performance Electric Drives").

6-2. Applicant is disclosing method and apparatus for testing the operation of an electronic unit by stimulating. The method steps include sending simulated input signals to said unit and receiving slow output signals from said unit by at least one microprocessor, receiving fast output signals in response to said simulated input signals by at least one programmable logic circuit, processing the fast output signals by the at least one programmable logic circuit to generate parameter values at a first frequency, storing said parameter values corresponding to said processed signals in a storing circuit; and accessing said stored parameter values by the at least one microprocessor at a second frequency which is slower than said first frequency and is compatible with an operating frequency of the microprocessor , wherein said at least one programmable logic circuit is of a FPGA type. The apparatus has the equivalent limitations. These features are generally disclosed in the prior art of record. However, the prior art of record, while generally disclosing these features, does not meet the conditions as suggested in MPEP section 2131, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."

In this application, the prior art of record does not disclose the specific sequence of steps or arrangement of elements in the apparatus as shown in Fig. 1 and disclosed within the context of independent claims 1 and 5. Therefore, Independent claims 1 and 5 have been allowed over the prior art of record.

Dependent claims 2-3 and 6-10 are allowable as they depend on the allowed independent claims 1 and 5 respectively.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kamini S. Shah can be reached on (571) 272-2279. The fax phone numbers for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day
September 18, 2006 H.D.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER